

Abstract

The present invention is to improve yield and reliability in a wiring step of a semiconductor device. When an Al wiring on an upper layer is connected through
5 an connection pillar onto an Al wiring on a lower layer embedded in a groove formed on an interlayer insulation film, a growth suppression film having an opening whose width is wider than that of the Al wiring is formed on the interlayer insulation film and the Al wiring. In
10 this condition, Al and the like are grown by a selective CVD method and the like. Accordingly, the connection pillar is formed on the Al wiring within the opening, in a self-matching manner with respect to the Al wiring.